



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Susumu INOUE

Application No.: 10/614,985

Filed: July 9, 2003

Docket No.: 116434

For: METHOD OF FABRICATING SEMICONDUCTOR DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

- ☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.
- ☒ 2. Relevance of the non-English language reference 31 is discussed in the present specification.
- ☒ 3. English-language Abstracts of the non-English language references 29-30 are attached hereto.

- ☒ 4. A computer-generated English translation of the following Japanese Patent Publications have been obtained from the website of the Japanese Patent Office ([<http://www.jpo.go.jp>]), and are attached, but have not been reviewed for accuracy. See References 28-30.

Respectfully submitted,



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Form PTO-1449 (REV. 8-83)		US Dept. of Commerce PATENT & TRADEMARK OFFICE		ATTY DOCKET NO. 116434		APPLICATION NO. 10/614,985	
				APPLICANT Susumu INOUE			
				FILING DATE July 9, 2003			
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)							
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	
	1	US 6,255,166 B1	07/03/2001	Ogura et al.			
	2	5,408,115	04/18/1995	Chang			
	3	5,969,383	10/19/1999	Chang et al.			
	4	5,422,504	06/06/1995	Chang et al.			
	5	5,494,838	02/27/1996	Chang et al.			
	6	US 6,177,318 B1	01/23/2001	Ogura et al.			
	7	US 6,248,633 B1	06/19/2001	Ogura et al.			
	8	10/636,582 Attorney Docket 116815	08/08/2003	Inoue			
	9	10/636,562 Attorney Docket 116817	08/08/2003	Inoue			
	10	10/689,990 Attorney Docket 117588	10/22/2003	Kasuya			
	11	10/636,581 Attorney Docket 116816	08/08/2003	Yamamukai			
	12	10/690,025 Attorney Docket 117576	10/22/2003	Kasuya			
	13	10/689,993 Attorney Docket 117577	10/22/2003	Kasuya			
	14	10/689,987 Attorney Docket 117575	10/22/2003	Kasuya			
	15	10/244,627 Attorney Docket 113761	09/17/2002	Ebina et al.			
	16	10/234,197 Attorney Docket 113668	09/05/2002	Ebina et al.			
	17	10/339,555 Attorney Docket 114656	01/10/2003	Shibata			
	18	10/350,010 Attorney Docket 114766	01/24/2003	Kasuya			
	19	10/349,943 Attorney Docket 114765	01/24/2003	Kasuya			
	20	10/234,095 Attorney Docket 113669	09/05/2002	Ebina et al.			
	21	10/052,255 Attorney Docket 111778	01/23/2002	Ebina et al.			
	22	10/052,549 Attorney Docket 111779	01/23/2002	Ebina et al.			
	23	10/244,623 Attorney Docket 113760	09/17/2002	Ebina et al.			
	24	10/350,075 Attorney Docket 114768	01/24/2003	Kasuya			
	25	10/342,307 Attorney Docket 114425	01/15/2003	Ueda			
	26	10/349,958 Attorney Docket 114767	01/24/2003	Kasuya			
	27	10/339,558 Attorney Docket 114655	01/10/2003	Inoue			

Date: December 8, 2003



FOREIGN PATENT DOCUMENTS					
		DOCUMENT NUMBER	DATE	COUNTRY	SUB CLASS
	28	JP B1 2978477 w/trans.	09/10/1999	Japan	
	29	JP A 7-161851 w/abstr. + trans.	06/23/1995	Japan	
	30	JP A 2001-156188 w/abstr. + trans.	06/08/2001	Japan	
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)					
	31	Hayashi et al., "Twin MONOS Cell with Dual Control Gates," IEEE Symposium on VLSI Technology Digest of Technical Papers, 2000			
	32	Chang et al., "A New SONOS Memory Using Source-Side Injection for Programming," IEEE Electron Device Letters, Vol 19, No. 7, pp. 253-255, July 1998			
	32	Chen et al., "A Novel Flash Memory Device with S Plit Gate Source Side Injection and ONO Charge Storage Stack (SPIN)," Symposium on VLSI Technology Digest of Technical Papers, pp. 63-64, 1997			
EXAMINER				DATE CONSIDERED	
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.					

Date: December 8, 2003